CV: Sergi Siso, February 2020

Research Interests

My research interests are in the field of High-Performance Computing (HPC), particularly in the portability of parallel software to modern architectures. Currently, my research focuses on how to leverage compiler-level techniques such as Domain Specific Languages (DSLs) and Dynamic Compilation to create performant and portable software abstractions between the application domain and the computational characteristics of applications (separation of concerns).

I have been the Principal Investigator of the Intel Parallel Computer Centre at Hartree Centre and the technical lead of a collaboration with Rolls-Royce aiming to port a FE application to many-core CPU architecture. Currently I am a contributor to the PSyclone code-generator open-source tool, I am an investigator in the EU EuroEXA project, and I am a member of the Intel eXtreme Performance User Group (IXPUG) steering committee.

The results of the mentioned work have been presented in international conferences and journals listed at the end of this document.

Experience

2015 – Present: Application Performance Engineer in the Hartree Centre (Science and Technology Facilities Council – UKRI) at Daresbury Laboratory.

My role is to analyse the performance of technical and scientific applications and adapt them to modern hardware architectures. During this period:

- I lead the Intel Parallel Computing Centre at Hartree Centre. I contributed to DualSPHysics (a smooth particle hydrodynamics to study free-surface flow phenomena.), DL_MESO (a mesoscale Lattice Boltzmann mesoscopic simulation package), LFRic (an Earth Weather and Climate modelling system) and leveraged OSPRay for visualizations.
- I lead a collaboration with Rolls-Royce to optimize an industrial Finite Elements solver for both inviscid and viscous compressible flows.
- I made several contributions to the PSyclone codebase. For instance, as part of the EuroEXA project, I developed an OpenCL back-end for the PSyclone that can target FPGA architectures.

2013 – 2013: Resident Student Researcher at Performance Tools Department, Barcelona Super-Computing Centre

Designed and implemented a software to process summarized profiling information from highly scalable applications and format such information in a way that the Dimemas software is able to simulate its performance in different systems. It was part of the CEPBA-tools toolchain.

2012 – 2013: Developer at SERIMAG MEDIA SL

Designed and implemented a document classifier application for a banking company. It uses data mining technologies such as Support Vector Machines and the Viterbi algorithm to classify a stream of incoming documents automatically.

2010 – 2011: Grant-holder cryptography researcher at Department of Cryptography and Graphs, University of LLeida

Designed and implemented an electronic voting system that works on different types of homomorphic cryptosystems, specifically over elliptic curves.

Education

2016 – Present: (Ongoing) PhD in Computer Sciences, Liverpool University

- Topic: Code generation techniques to inject Dynamic Optimizations to HPC applications.
- Supervisor: Jeyan Thiyagalingam
- Funded by Hartree Centre

2013 – 2014: MSc with Distinction in High Performance Computing, EPCC, University of Edinburgh

- Scholarship: "Highly Skilled Workforce" award of the Scottish Funding Council.
- Dissertation: "Parallelisation of the Coupled Coherent States quantum dynamics simulation" | Advisor: Andrew Turner

2012 – 2013: Master's Degree in Information Technology, Polytechnic University of Catalonia

- Thesis: "Simulating parallel systems using summarized application information" | Advisor: Jesus Labarta

2008 – 2012: Bachelor's Degree with Honours in 'Enginyeria Tecnica en Informatica de Sistemes' (Technical Computer Engineering), University of LLeida

- Thesis: "Electronic voting system over elliptic curve cryptography" | Advisor: J.M Miret

Selected Publications and Presentations

Sergi Siso, Wes Armour, and Jeyarajan Thiyagalingam (2019) Evaluating Auto-Vectorizing Compilers through Objective Withdrawal of Useful Information. ACM Transactions on Architecture and Code Optimization (TACO). 16, 4, Article 40 (October 2019).

SC'16 Tutorial: Debugging and Performance Analysis on Native and Offload HPC Architectures, Conference Tutorial, Supercomputing Conference (SC16), Salt Lake City (USA), 2016

Ashworth M., Meng J., Novakovic V., Siso S. (2016) Early Application Performance at the Hartree Centre with the OpenPOWER Architecture. In: Taufer M., Mohr B., Kunkel J. (eds) High Performance Computing. ISC High Performance 2016. Lecture Notes in Computer Science, vol 9945. Springer, Cham

Sergi Siso, Luke Mason, Michael Seaton (2016) Code modernization of DL_MESO LBE to achieve good performance on the Intel Xeon Phi. Proceedings of EMerging Technology (EMiT) Conference 2016

Sergi Siso, DualSPHysics Performance on Intel Xeon Phi, Society for Industrial and Applied Mathematics (SIAM) Parallel Processing Conference, Paris, 2016

ISC'15 Tutorial: The Road to Application Performance on Intel Xeon Phi, DL_MESO Lattice Boltzmann Data Layout, Conference Tutorial, International Supercomputing Conference (ISC15), Frankfurt (Germany), 06/2015